WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising a plurality of memory banks each having rows that can be activated independently of another memory bank, wherein

where N is a natural number equal to or greater than two and M is a natural number equal to or greater than two and equal to or smaller than N–1,

a first memory bank of said plurality of memory banks includes first to N-th sub-memory blocks,

an M-th sub-memory block of said first to N-th sub-memory blocks includes

a first memory cell array including a plurality of memory cells arranged in rows and columns and

a first local control circuit, in a refresh mode, starting an operation of successively selecting rows of said first memory cell array in response to a first refresh end signal received from an (M–1)th sub-memory block and instructing a refresh start to an (M+1)th sub-memory block when said operation of successively selecting rows ends, and

said first memory bank further includes a plurality of sense amplifier bands each shared by adjacent two of said first to N-th sub-memory blocks.

2. The semiconductor memory device according to claim 1 wherein

each of said first to N-th sub-memory blocks includes a plurality of word lines for performing row selection for a memory cell,

said semiconductor memory device further comprising:

an address counter generating a refresh address for use in common in said first to N-th sub-memory blocks to select one of said plurality of word lines; and

an address bus transmitting said refresh address to said first to N-th sub-memory blocks.

3. The semiconductor memory device according to claim 1 wherein said M-th sub-memory block includes first to K-th word lines for performing row selection for a memory cell, where K is a natural number equal to or greater than two, and

said first local control circuit includes

a row address decoder activated in response to the first refresh end signal received from the (M−1) sub-memory block for decoding a refresh address to select one of said first to K-th word lines and

a refresh end detection circuit outputting a second refresh end signal to instruct a refresh start to said (M+1)th sub-memory block when said refresh address corresponds to a refresh end of said K-th word line.

4. The semiconductor memory device according to claim 1 wherein said first sub-memory block includes

a second memory cell array including a plurality of memory cells arranged in rows and columns and

a second local control circuit, in a refresh mode, starting an operation of successively selecting rows of said second memory cell array in response to a third refresh end signal received from the N-th sub-memory block and instructing a refresh start to a second sub-memory block when said operation of successively selecting rows of said second memory cell array ends.

5. The semiconductor memory device according to claim 4 wherein said first local control circuit includes a first refresh start control circuit inactivated in response to a reset signal and activated in response to said first refresh end signal received from said (M−1)th sub-memory block for outputting a first refresh start signal, and

said second local control circuit includes a second refresh start control circuit activated in response to said reset signal and activated in response to said third refresh end signal received from said N-th sub-memory block for outputting a second refresh start signal.

6. A semiconductor memory device comprising a first memory block, wherein

said first memory block includes a plurality of sub-memory blocks being refreshed in a circulating manner in a refresh mode,

each of said plurality of sub-memory blocks includes

a memory cell array including a plurality of memory cells arranged in rows and columns and

a local control circuit performing an operation of successively selecting rows of said memory cell array in response to an end of a refresh operation in a sub-memory block at a previous stage which precedes by one in refresh-circulating order of said plurality of sub-memory blocks, and

a refresh cycle period in each of said plurality of memory blocks is determined depending on a number of said sub-memory blocks included in said first memory block.

7. The semiconductor memory device according to claim 6 wherein

said local control circuit corresponding to at least one of said plurality of sub-memory blocks includes a gate circuit activating a refresh start signal in response to a refresh end signal from a corresponding sub-memory block at a previous stage and inactivating said refresh start signal in response to a refresh stop signal,

said semiconductor memory device further comprising a second memory block holding a refresh operation irrespective of said refresh stop signal in said refresh mode.